

WHAT IS CLAIMED IS:

1 1. For use in a processor, an instruction handling
2 system for determining instruction folding comprising:

3 at least one fold decoder associated with an
4 instruction fetch buffer stack,

5 the at least one fold decoder coupled to a set of
6 successive entries within the instruction fetch buffer
7 stack and examining contents within the successive entries
8 prior to a main decode of the contents within the
9 successive entries to determine whether the successive
10 entries contain two or more instructions which may be
11 folded,

12 the at least one fold decoder generating fold-
13 status information for the contents within the successive
14 entries indicating whether the successive entries contain
15 two or more instructions which may be folded.

1 2. The instruction handling system as set forth in
2 Claim 1 wherein the at least one fold decoder further
3 comprises:

4 a plurality of fold decoders associated with the
5 instruction fetch buffer stack and including the at least
6 one fold decoder,

7 each fold decoder coupled to a different set of
8 successive entries within the instruction fetch buffer
9 stack, wherein the different sets of successive entries
10 overlap, and examining contents within a corresponding set
11 of successive entries to determine whether the
12 corresponding set of successive entries contain two or more
13 instructions which may be folded,

14 each fold decoder generating fold-status
15 information for the contents within the corresponding set
16 of successive entries indicating whether the corresponding
17 set of successive entries contain two or more instructions
18 which may be folded.

1 3. The instruction handling system as set forth in
2 Claim 2 wherein the fold-status information produced by
3 each fold decoder includes a number of instructions which
4 may be folded and a size of each instruction which may be
5 folded.

1 4. The instruction handling system as set forth in
2 Claim 2 wherein the fold-status information for each set of
3 successive entries is stored in association with the
4 respective set of successive entries within the instruction
5 fetch buffer stack.

1 5. The instruction handling system as set forth in
2 Claim 1 wherein the at least one fold decoder checks the
3 contents within the successive entries for instructions of
4 a variable size and for possible folding of a variable
5 number of instructions.

1 6. The instruction handling system as set forth in
2 Claim 1 further comprising:

3 a decoder receiving the fold-status information
4 together with the contents of the successive entries for
5 translation of the contents of the successive entries into
6 signals which may be operated on by an execution unit.

1 7. The instruction handling system as set forth in
2 Claim 1 wherein the decoder employs the fold-status
3 information during folding of at least the contents of the
4 successive entries into a single operation.

1 8. A processor comprising:

2 an instruction fetch mechanism retrieving
3 instructions for storage within an instruction fetch
4 buffer;

5 an instruction decode mechanism for translating
6 instructions into signals which may be operated on by at
7 least one execution unit; and

8 an instruction handling system coupled between
9 the instruction fetch buffer and instruction decode
10 mechanism for determining instruction folding comprising:

11 at least one fold decoder associated with an
12 instruction fetch buffer stack,

13 the at least one fold decoder coupled to a
14 set of successive entries within the instruction fetch
15 buffer stack and examining contents within the
16 successive entries prior to a main decode of the
17 contents within the successive entries to determine
18 whether the successive entries contain two or more
19 instructions which may be folded,

20 the at least one fold decoder generating
21 fold-status information for the contents within the
22 successive entries indicating whether the successive
23 entries contain two or more instructions which may be
24 folded.

1 9. The processor as set forth in Claim 8 wherein the
2 at least one fold decoder further comprises:

3 a plurality of fold decoders associated with the
4 instruction fetch buffer stack and including the at least
5 one fold decoder,

6 each fold decoder coupled to a different set of
7 successive entries within the instruction fetch buffer
8 stack, wherein the different sets of successive entries
9 overlap, and examining contents within a corresponding set
10 of successive entries to determine whether the
11 corresponding set of successive entries contain two or more
12 instructions which may be folded,

13 each fold decoder generating fold-status
14 information for the contents within the corresponding set
15 of successive entries indicating whether the corresponding
16 set of successive entries contain two or more instructions
17 which may be folded.

1 10. The processor as set forth in Claim 9 wherein the
2 fold-status information produced by each fold decoder
3 includes a number of instructions which may be folded and a
4 size of each instruction which may be folded.

1 11. The processor as set forth in Claim 9 wherein the
2 fold-status information for each set of successive entries
3 is stored in association with the respective set of
4 successive entries within the instruction fetch buffer
5 stack.

1 12. The processor as set forth in Claim 8 wherein the
2 at least one fold decoder checks the contents within the
3 successive entries for instructions of a variable size and
4 for possible folding of a variable number of instructions.

1 13. The processor as set forth in Claim 8 wherein the
2 instruction decode mechanism receives the fold-status
3 information together with the contents of the successive
4 entries.

1 14. The processor as set forth in Claim 8 wherein the
2 instruction decode mechanism employs the fold-status
3 information during folding of at least the contents of the
4 successive entries into a single operation.

1 15. For use in a processor, a method of determining
2 instruction folding comprising:

3 prior to decoding contents within a set of
4 successive entries within an instruction fetch buffer
5 stack,

6 examining the contents within the successive
7 entries to determine whether the successive entries
8 contain two or more instructions which may be folded;
9 and

generating fold-status information for the
contents within the successive entries indicating
whether the successive entries contain two or more
instructions which may be folded.

1 16. The method as set forth in Claim 15 wherein the
2 step of examining the contents within the successive
3 entries to determine whether the successive entries contain
4 two or more instructions which may be folded further
5 comprises:

6 examining contents within each of a different set
7 of successive entries within the instruction fetch buffer
8 stack, wherein the different sets of successive entries
9 overlap, to determine whether the corresponding set of
D successive entries contain two or more instructions which
E may be folded.

1 17. The method as set forth in Claim 16 wherein the
2 step of generating fold-status information for the contents
3 within the successive entries indicating whether the
4 successive entries contain two or more instructions which
5 may be folded further comprises:

6 generating fold-status information for the
7 contents within each set of successive entries indicating
8 whether the corresponding set of successive entries contain
9 two or more instructions which may be folded, wherein the
10 fold-status information includes a number of instructions
11 which may be folded and a size of each instruction which
12 may be folded.

1 18. The method as set forth in Claim 16 further
2 comprising:

3 storing the fold-status information for each set
4 of successive entries in association with the respective
5 set of successive entries within the instruction fetch
6 buffer stack.

1 19. The method as set forth in Claim 15 wherein the
2 step of examining contents within each of a different set
3 of successive entries within the instruction fetch buffer
4 stack further comprises:

5 checking the contents within the successive
6 entries for instructions of a variable size and for
7 possible folding of a variable number of instructions.

1 20. The method as set forth in Claim 15 further
2 comprising:

3 transmitting the fold-status information together
4 with the contents of the successive entries to an
5 instruction decoder translating the contents of the
6 successive entries into signals which may be operated on by
7 an execution unit; and

8 employing the fold-status information during
9 folding of at least the contents of the successive entries
10 into a single operation within the instruction decoder.